



FIG. 1 (Prior Art)

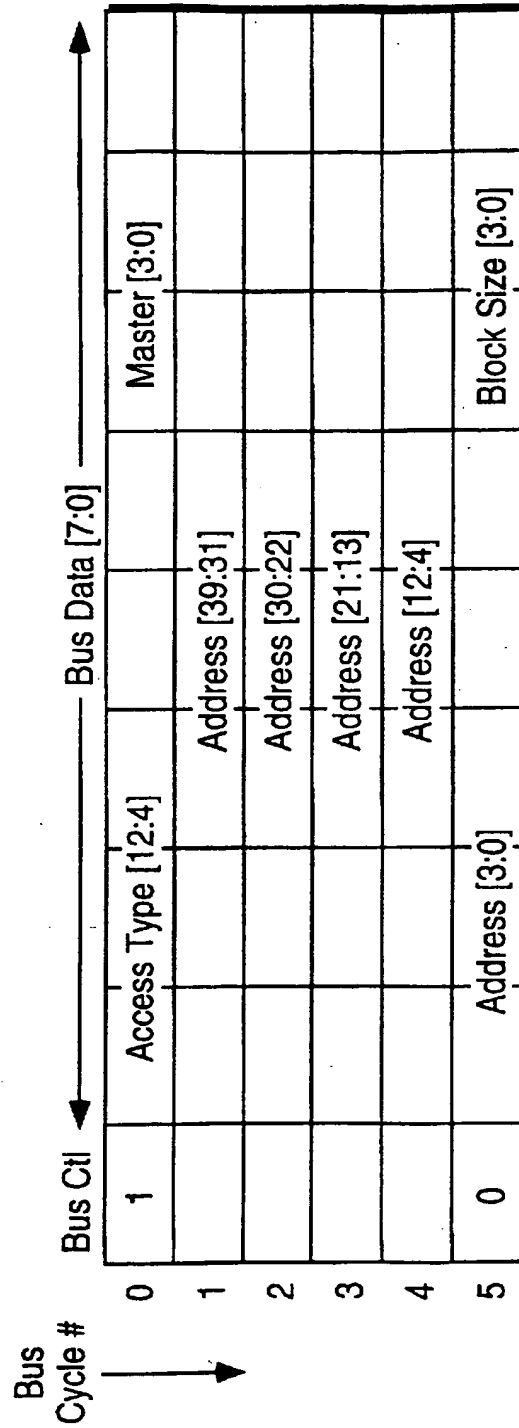




FIG. 2

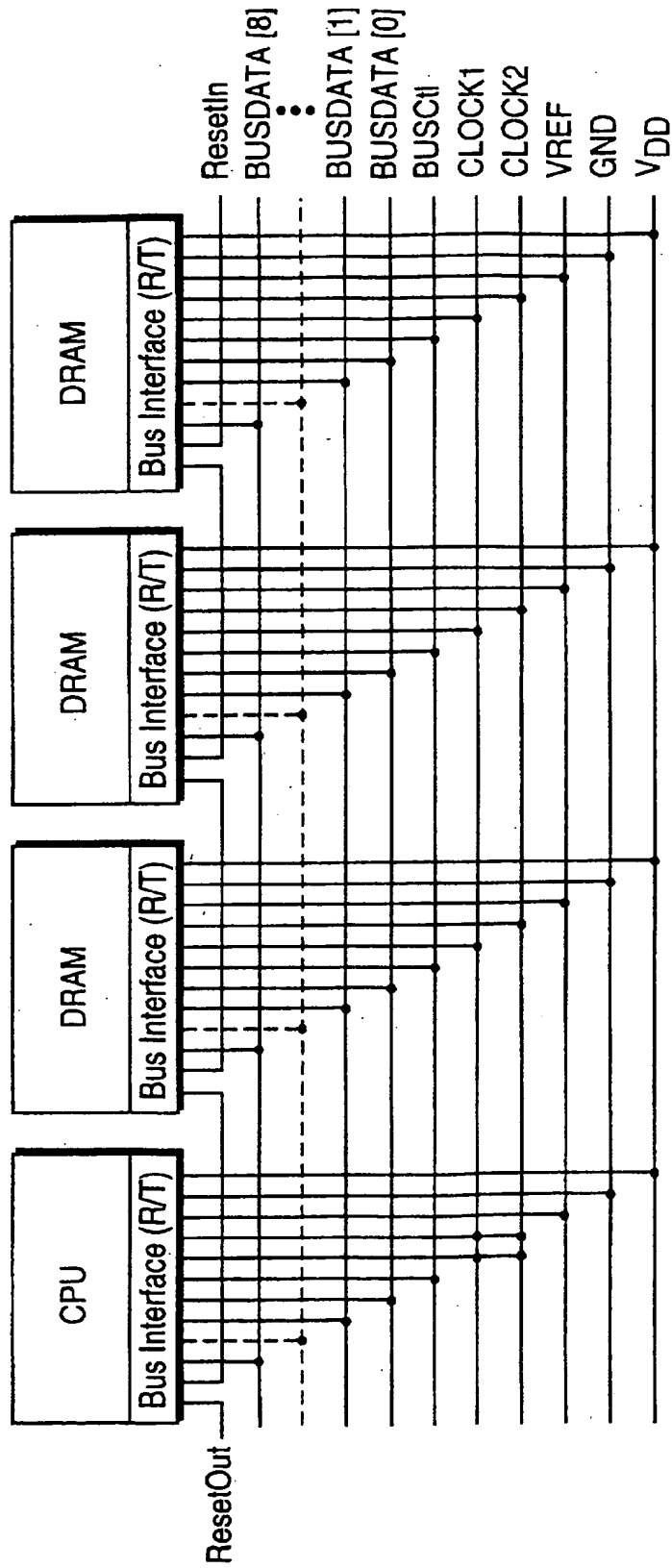




FIG. 3

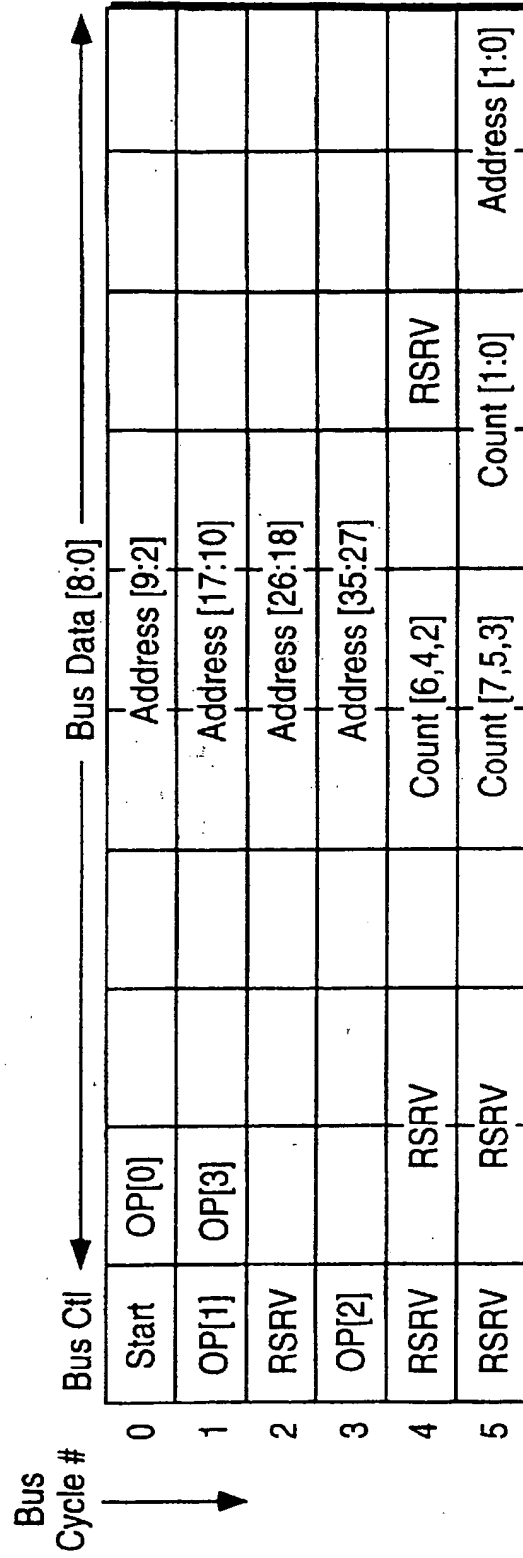




FIG. 4

Bus Cycle #	Bus Ctl	Bus Data [8:0]					
0	Start	OP[0]			Address [9:2]		
1	OP[1]	OP[3]			Address [17:10]		
2	C/D				Address [26:18]		
3	OP[2]				Address [35:27]		
4	C/D		Master [3:2]		Count [6,4,2]	RSRV	
5	RSRV		Master [1:0]		Count [7,5,3]	Count [1:0]	Address [1:0]

FIG. 5a

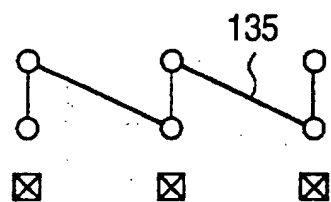
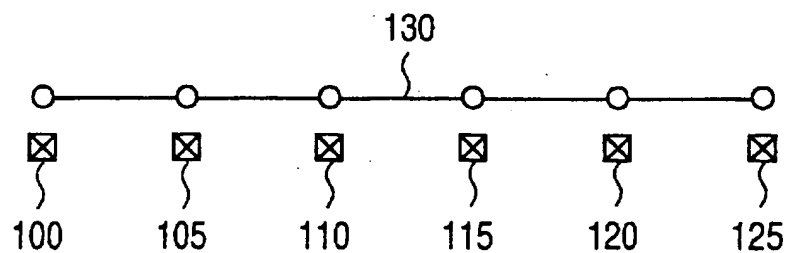


FIG. 5b

FIG. 6a

Adr[1:0]	Mask[3:0]
00	1111
01	1110
10	1100
11	1000

FIG. 6b

Count[1:0]	Mask[7:4]
00	0001
01	0011
10	0111
11	1111



FIG. 7a

One Byte Transfer (MasterCount[7:0] = 00000000)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
000000	00	00	0001	1111	0001
000000	01	01	0011	1110	0010
000000	10	10	0111	1100	0100
000000	11	11	1111	1000	1000

FIG. 7b

Two Byte Transfer (MasterCount[7:0] = 00000001)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
000000	01	00	0011	1111	0011
000000	10	01	0111	1110	0110
000000	11	10	1111	1100	1100
000001	00	11	0001	1000	not used- two QB's



# FIG. 7c

Four Byte Transfer (MasterCount[7:0] = 00000011)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
000000	11	00	1111	1111	1111
000001	00	01	0001	1110	not used- two QB's
000001	01	10	0011	1100	not used- two QB's
000001	10	11	0111	1000	not used- two QB's

# FIG. 7d

Eight Byte Transfer (MasterCount[7:0] = 00000111)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
000001	11	00	1111	1111	not used- two QB's
000010	00	01	0001	1110	not used- three QB's
000010	01	10	0011	1100	not used- three QB's
000010	10	11	0111	1000	not used- three QB's